Syllabus for BIOE166-01: Bioelectronics

Fall 2021
Instructor: Sushma Shrinivasan

Designation:	Upper Division
Catalog Description:	This course is intended for the upper division engineering students to facilitate the student's development into bioengineering investigation. The course has been designed to introduce fundamental principles of analog and digital electronics and it's application to bioengineering. The course will provide the background to design electronic instrumentation to assess physiological and molecular functions, from bioelectrical measurements to spectroscopic detection.
Text Books and Other Required Materials:	Microelectronic Circuits by Sedra/Smith, 8th Edition Digital Design by Morris Mano and Michael Ciletti, 6th Edition Instructor notes will be provided as additional course material.
Course Objectives/ Student Learning Outcomes:	By the end of this course, students will be able to: 1. To understand the basic concepts of solid state physics applied to semiconductors. 2. To learn how to design circuits with operational amplifier. 3. To understand the implementation of digital algebra using logic circuits.
Program Learning Outcomes:	
Prerequisites by Topic:	BIOE 065 Bio Circuit Theory
Course Policies:	Homeworks are typically assigned on Wednesday (check CatCourses) and will be due (via catcourse) on the date indicated (typically after one week). Late homeworks will be accepted till the following day (basically a 24-hour extension) but for a reduced credit of 75%. To iterate, feel free to discuss among yourselves to complete the homework problems, but reproducing another person's work is not acceptable. Syllabus for the exams will be announced in class as the course progresses. Review sessions may be held before the exams. Quizzes (~ 3) will be conducted. Make sure to stay updated with catcourse on course announcements/material posted. Any material that is posted is only for your benefit and should not be shared or posted online by you.
Academic Dishonesty Statement:	a. Each student in this course is expected to abide by the University of California, Merced's Academic Honesty Policy. Any work submitted by a student in this course for academic credit will be the student's own work. b. You are encouraged to study together and to discuss information and concepts covered in lecture and the sections with other students. You can give "consulting" help to or receive "consulting" help from such students. However, this permissible cooperation should never involve one student having possession of a copy of all or part of work done by someone else, in the form of an e mail, an e mail attachment file, a diskette, or a hard copy. Should copying occur, both the student who copied work from another student and the student who gave material to be copied will both automatically receive a zero for the assignment. Penalty for

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violation of this Policy can also be extended to include failure of the course and University disciplinary action.
c. During examinations, you must do your own work. Talking or discussion is not permitted during the examinations, nor may you compare papers, copy from others, or collaborate in any way. Any collaborative behavior during the examinations will result in failure of the exam, and may lead to failure of the course and University disciplinary action.

Disability Statement: Accommodations for Students with Disabilities: The University of California Merced is committed to ensuring equal academic opportunities and inclusion for students with disabilities based on the principles of independent living, accessible universal design and diversity. I am available to discuss appropriate academic accommodations that may be required for student with disabilities. Requests for academic accommodations are to be made during the first three weeks of the semester, except for unusual circumstances. Students are encouraged to register with Disability Services Center to verify their eligibility for appropriate accommodations.

Topics:

1. SEMICONDUCTORS DEVICES I.
Solid State Physics. Electrons and holes. The P-N junction. Diodes. Diodes as thermosensors. Photodiodes. Avalanche effect. Avalanche effect diode. Bipolar Transistors. PNP and NPN junctions. Base, collector and emitter.

2. SEMICONDUCTORS DEVICES II.
H parameters equivalent circuit. Common emitter amplifier. DC behavior: the load slope and the Q point. AC behavior. Emitter follower amplifier. Field effect transistors: JFET and MOSFET. Source, Drain and Gate.

3. OPERATIONAL AMPLIFIERS: DC PERFORMANCE I.
The operational amplifier. Input resistance. Output resistance. Open loop gain. Bias currents. Offset currents. Offset voltage. Differential mode gain. Common mode gain. Common mode rejection ratio. Negative feedback. Open loop gain and closed loop gain.

4. OPERATIONAL AMPLIFIERS: DC PERFORMANCE II.
Inverter amplifier. Addition amplifier. Non-inverter amplifier. The voltage follower. Transimpedance amplifier (Current to voltage converter). Howland pump. Differential amplifier.

5. OPERATIONAL AMPLIFIERS: AC AND TRANSIENT PERFORMANCE I.
Frequency response. Bode Plot. Stability. Barkhausen s criteria. Phase margin and amplitude margin.

6. OPERATIONAL AMPLIFIERS: AC AND TRANSIENT PERFORMANCE II.
Differentiator amplifier. Integrator amplifier. Logarithmic amplifier. Transient response.

7. POWER SUPPLIES.
Rectification. Half wave and full wave. Filters. Low pass filters. High pass Filters.

8. DIGITAL TECHNIQUES: PRINCIPLES.
Numbering systems. Binary, octal and hexadecimal numbers. Boolean algebra.

Designation:	Upper Division Conversion and operations. AND gate. OR gate. Inverter. NAND gate. NOR gate. Exclusive OR gate. Morgan s laws. Logic families. TTL and CMOS. 9. DIGITAL TECHNIQUES: COMBINATIONAL CIRCUITS. Truth tables. Karnough s diagram. Minterm addition. Maxterm product. Synthesis of combinational circuits. Logic comparators. Codifiers. Decodifiers. Multiplexers. 10. DIGITAL TECHNIQUES: SEQUENCIAL CIRCUITS. Monostable oscillator. Bistable oscillator. Astable oscillator. The MC555. The Flip-Flop . Flip Flop (FF) types: RS type. JK FF. JK FF Master slave. D FF. T FF. Level detector and slope detector. Counters. Shift registers. 11. MEMORIES Structure: address and data bus. ROM, PROM, EPROM and flash RAM. Volatiles Memories: RAM, SRAM and DRAM. Addressing modes. 12. Bioconcepts Measurements of membrane potential. Measurements of transmembrane currents. The Patch Clamp amplifier.The voltage clamp method. Two electrode voltage clamp. Cut open oocytes clamp.
Class/laboratory Schedule:	Monday & Wednesday 3-4:15 pm SSM 104 ; No labs
Midterm/Final Exam Schedule:	Midterm 1: Tentative date Oct 4th,SSM 104 Midterm 2: Tentative date Nov 8th,SSM 104 Finals: Dec 15th, 8:00-11:00am, SSM 104 Quizzes: Quiz 1: Tentative date : Sep 27th (syllabus covered up to and including Sept 22nd lecture). Quiz 2:Tentative date : Nov 1st (syllabus covered up to and including Oct 27th lecture). Quiz 3: Tentative date : Dec 6th (syllabus covered up to and including Dec 1st lecture).
Course Calendar:	
Professional Component:	
Assessment/Grading Policy:	Homework- 15% Midterm 1- 25% Midterm 2- 25% In-class quiz- 5% Finals- 30%
Coordinator:	Prof. Sushma Shrinivasan
Contact Information:	Email: sshrinivasan@ucmerced.edu
Office Hours:	Instructor: Monday & Wednesday; 1:30-2:30pm via zoom (zoom link will be posted in catcourse announcement) or by appointment.